In the Claims

Please amend Claim 1 as follows:

Subt B'

1. (Amended) An electrostatic discharge protection device comprising:

a p-well region in a semiconductor substrate;

an n+ region in said p-well region wherein said n+ region is connected to a first voltage supply;

an n-well region in said p-well region wherein said n+ region is spaced from said n-well region a distance such that a depletion region extends therebetween during normal operation; and

a p+ region in said n-well region wherein said p+ region is connected to a second voltage supply of greater value than said first voltage supply during said normal operation wherein current is conducted through said n+ region to said p+ region during an electrostatic discharge event, wherein said n-well region is not otherwise connected, and wherein no MOS gate is formed within said device.

Please amend Claim 8 as follows:

Subt B2

8. (Amended) An electrostatic discharge protection device comprising:

a p-well region in a semiconductor substrate;

an n+ region in said p-well region wherein said n+ region is connected to a first voltage supply;

an n-well region in said p-well region wherein said n+ region is spaced from said n-well region a distance such that a depletion region extends therebetween during normal operation and wherein said distance between said n+ region and said n-well region is between about 0.2 microns and 1.0 microns; and

a p+ region in said n-well region wherein said p+ region is connected to a second voltage supply of greater value than said first voltage supply during said normal operation wherein current is conducted through said n+ region to said p+ region during an electrostatic discharge event, wherein said n-well region is not otherwise connected, and wherein no MOS gate is formed within said device.

Please amend Claim 14 as follows:

14. (Amended) An electrostatic discharge protection circuit on an integrated circuit device comprising:

a ground pad connected to an external ground reference and to a p+ region in a p-well in a substrate;

a first voltage supply pad connected to an external first voltage supply and to an n+ region in said p-well; and

a second voltage supply pad connected to an external second voltage supply of greater value than said external first voltage supply during normal operation and to a p+ region in an n-well region in said p-well region wherein said n+ region is spaced from said n-well region a distance such that a depletion region extends therebetween during said normal operation, wherein current is conducted through said external second voltage supply pad to said external first voltage supply pad during an electrostatic discharge event, wherein said n-well region is not otherwise connected, and wherein no MOS gate is formed within said device.